CMS1650 User Manual

LED driver control/keyboard scanning ASICs

Rev. 1.3.0

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1. Product Description

1.1 General description

The CMS1650 is a specialized integrated circuit for LED (Light Emitting Diode) driving control with a keyboard scanning interface. It internally integrates MCU I/O control digital interfaces, data latches, LED drivers, keyboard scanning, and brightness adjustment circuits. The CMS1650 offers stable performance, reliable quality, and strong anti-interference capabilities, making it suitable for applications requiring 24-hour, long-term continuous operation.

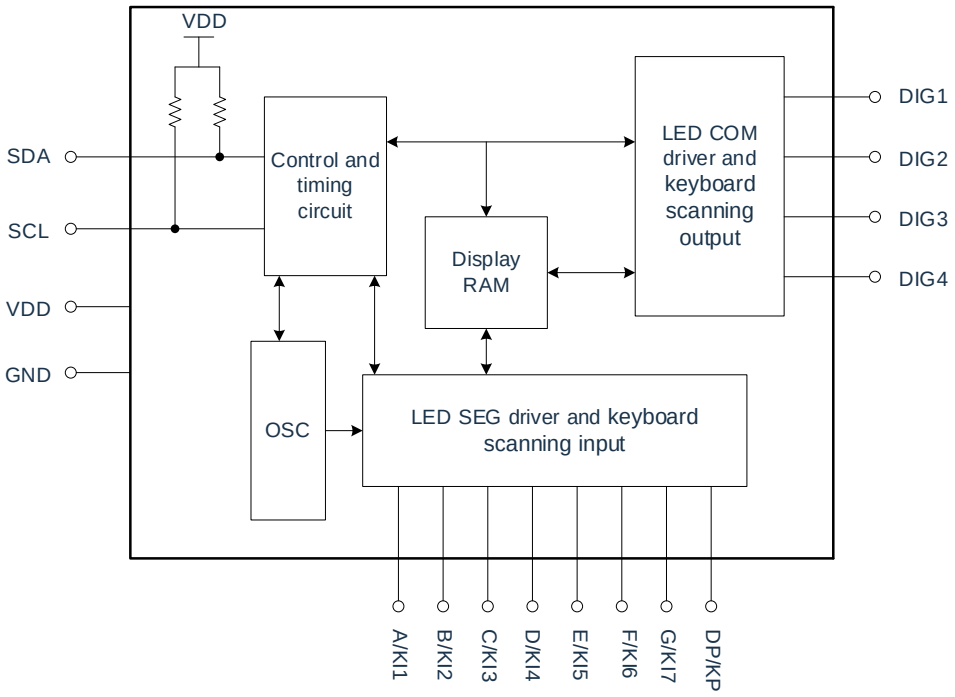
1.2 Features

- Two LED display modes: 8SEG×4COM and 7SEG×4COM
- SEG drive current > 25mA, COM drive current > 150mA
- Supports 8 levels of brightness control
- Keyboard scanning: 7×4bit with an internally integrated BJT driver
- High speed two-wire serial interface
- Built in clock oscillation circuit
- Built in power on reset circuit
- Supports 2.8V to 5.5V supply voltage
- Package form: DIP16, SOP16

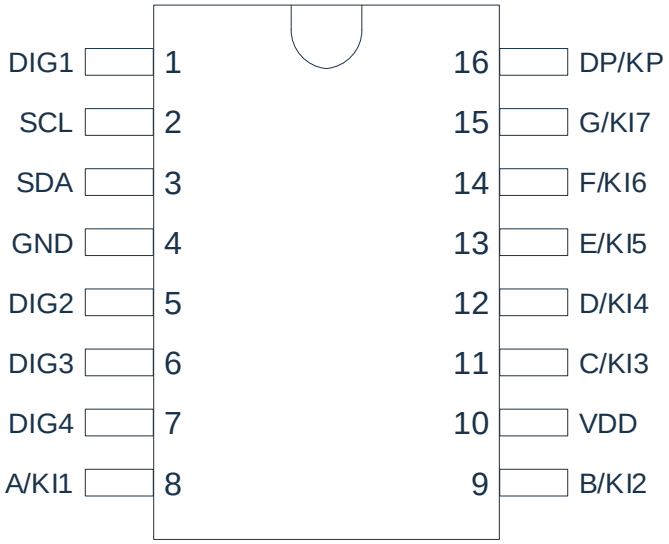
1.3 Applications

Display drivers for household appliances such as set-top boxes, air conditioners, DVD/VCD players, etc.

1.4 System structure diagram



1.5 Pinouts



CMS1650 pin description:

Pin name	Pin number	I/O	Description
DIG1	1	O	LED COM driver output 1/Keyboard scanning output 1
DIG2	5	O	LED COM driver output 2/Keyboard scanning output 2
DIG3	6	O	LED COM driver output 3/Keyboard scanning output 3
DIG4	7	O	LED COM driver output 4/Keyboard scanning output 4
SCL	2	I	Clock input
SDA	3	O/I	Data input/output
A/KI1	8	O/I	LED SEG driver output A/Keyboard scanning input KI1
B/KI2	9	O/I	LED SEG driver output B/Keyboard scanning input KI2
C/KI3	11	O/I	LED SEG driver output C/Keyboard scanning input KI3
D/KI4	12	O/I	LED SEG driver output D/Keyboard scanning input KI4
E/KI5	13	O/I	LED SEG driver output E/Keyboard scanning input KI5
F/KI6	14	O/I	LED SEG driver output F/Keyboard scanning input KI6
G/KI7	15	O/I	LED SEG driver output G/Keyboard scanning input KI7
DP/KP	16	O	LED SEG output DP/Keyboard flag output KP
GND	4	-	Logic ground
VDD	10	-	Logic power supply

2. Communication Protocol

The CMS1650 communicates using a 2-wire serial transmission protocol.

1) Start signal (START)/Stop signal (STOP)
   - Start signal: a transition of SDA from a high to a low state while SCL is high. Such as (Figure 2-1) paragraph A.
   - Stop signal: a transition of SDA from a low to a high state while SCL is high. Such as (Figure 2-1) paragraph E.
2) ACK signal

   If the communication is successful, after the 8th clock falling edge in serial communication, the CMS1650 will actively pull the SDA line low. It will hold this state until the rising edge of the SCL is detected, at which point the SDA line will be released to an input state (for the chip), as shown in (Figure 3) paragraph D.
3) Write 1 and 0
   - Write 1: a transition of SCL from a low to a high state and then from a high to a low state while SDA is high. See (Figure 2-1) paragraph B.
   - Write 0: a transition of SCL from a low to a high state and then from a high to a low state while SDA is low. See (Figure 2-1) paragraph C.

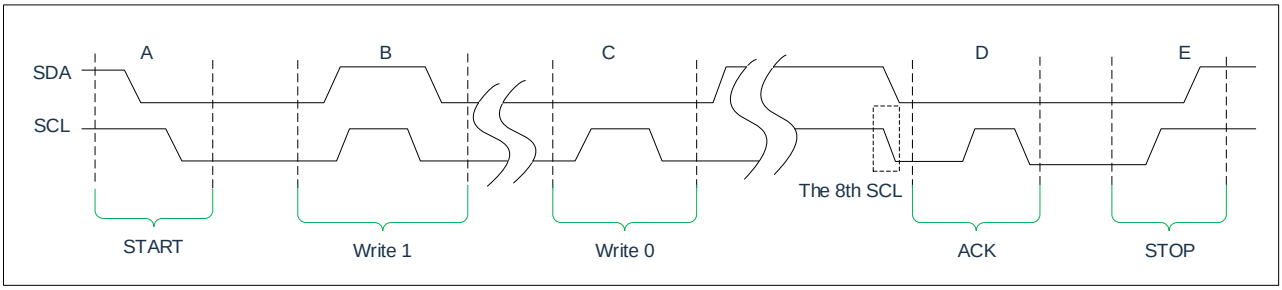


Figure 2-1: CMS1650 communicate protocol

4) One-byte data transmission format

   The data transmission format for one byte is shown in Figure 4, with MSB sent first and LSB last. The microprocessor communicates with the CMS1650 via a two-wire bus interface. During data input, when SCL is high, the signal on SDA must remain unchanged; the signal on SDA can only change when the SCL clock signal is low. The start condition for data input is when SDA transitions from high to low while SCL is high. The stop condition is when SDA transitions from low to high while SCL is high.

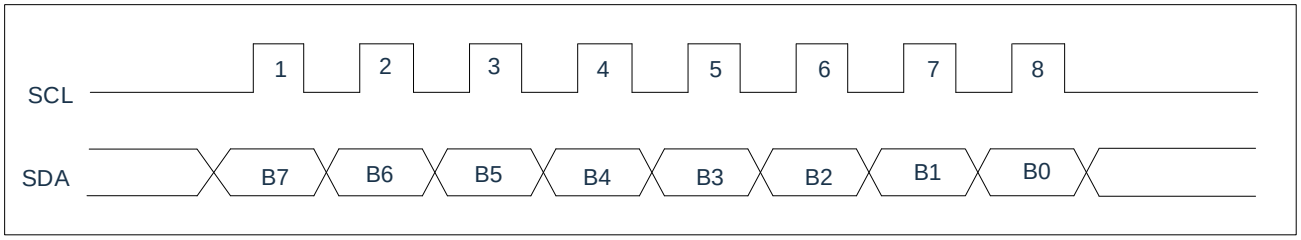


Figure 2-2: Data transmission format

5) Read key data timing

The data is read at the falling edge of SCL and output from the CMS1650 SDA pin.

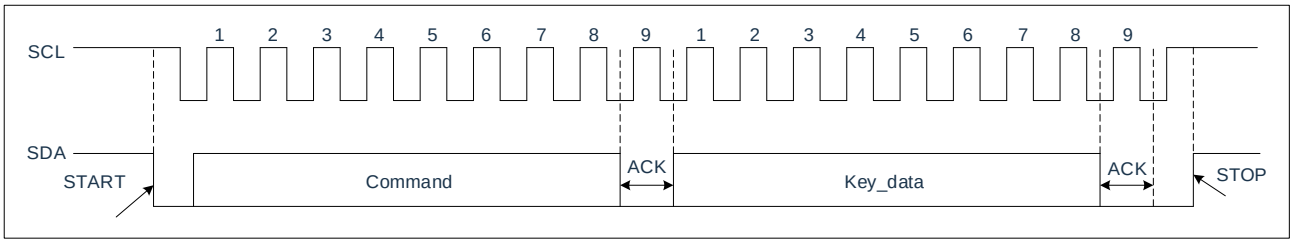


Figure 2-3: Read key data timing

Command: Send the read key command.

Key_data: The read keyboard scan code.

3. Keyboard Scan Code

CMS1650 corresponding keyboard scan code:

Address	DIG4	DIG3	DIG2	DIG1
A/KI1	47H	46H	45H	44H
B/KI2	4FH	4EH	4DH	4CH
C/KI3	57H	56H	55H	54H
D/KI4	5FH	5EH	5DH	5CH
E/KI5	67H	66H	65H	64H
F/KI6	6FH	6EH	6DH	6CH
G/KI7	77H	76H	75H	74H

Note: When reading keys, a 2kΩ resistor is connected in series with DIG and KI. Combination keys are not supported.

4. Control Command

1) Data command settings

B7	B6	B5	B4	B3	B2	B1	B0	Description
0	1	0	0	1	0	0	0	Mode command
0	1	0	0	1	X	X	1	Read key data command

Note: The “X” bit in the table can be either 1 or 0; it is recommended to write 0. Other bits must have fixed values.

2) Display command settings

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0	Function	Description
X	0	0	0		X	X		Brightness setting	Level 8 brightness
X	0	0			X	X			Level 1 brightness
X	0	1	0		X	X			Level 2 brightness
X	0	1	1		X	X			Level 3 brightness
X	1	0	0		X	X			Level 4 brightness
X	1	0	1		X	X			Level 5 brightness
X	1	1	0		X	X			Level 6 brightness
X	1	1	1		X	X			Level 7 brightness
X				0	X	X			8-segment display mode
X				1	X	X			7-segment display mode
X					X	X	0	ON/OFF display bit	OFF
X					X	X	1		ON

Note: The “X” bit in the table can be either 1 or 0; it is recommended to write 0.

5. Display RAM Address

This register stores data transmitted to the CMS1650 from external devices via the serial interface. It contains 4-byte units, each corresponding to the LED lights connected to the chip's A/KI~DP/KP and DIG pins, as allocated in the figure below:

When writing LED display data, operate from the high to low address and from the high to low bits of the data byte.

A/KI1	B/KI2	C/KI3	D/KI4	E/KI5	F/KI6		G/KI7	DP/KP	
xxHL (the low four bits)					xxHU (the high four bits)				
B0	B1	B2	B4	B5	B6		B7	B8	
68HL					68HU				DIG1
6AHL					6AHU				DIG2
6CHL					6CHU				DIG3
6EHL					6EHU				DIG4

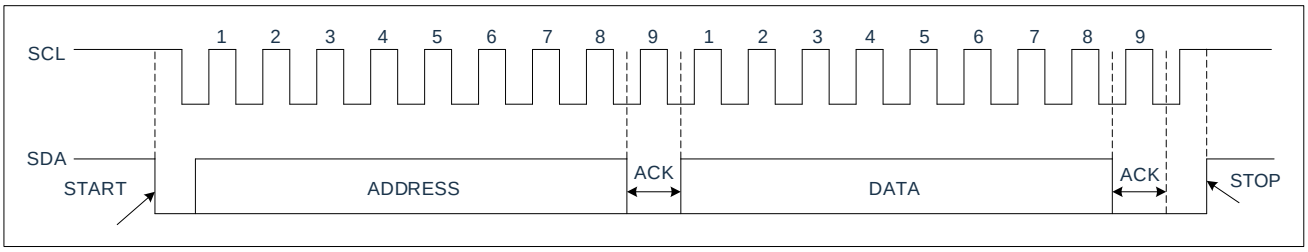
1) Display RAM address command

MSB LSB

B7	B6	B5	B4	B3	B2	B1	B0	RAM address
0	1	1	0	1	0	0	0	68H
0	1	1	0	1	0	1	0	6AH
0	1	1	0	1	1	0	0	6CH
0	1	1	0	1	1	1	0	6EH

Note: This instruction is used to set the address of the display register.

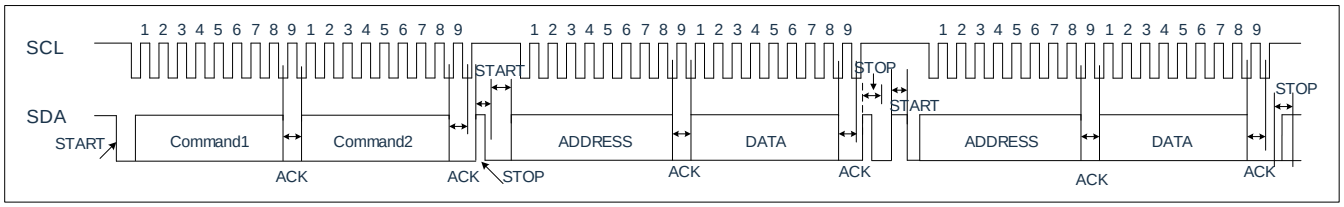
2) Timing for writing data to the display memory address



ADDRESS: Write the display memory address to the CMS1650.

DATA: Write the data to be displayed to the CMS1650.

5.1 A complete write display timing



Command1: Data command: 48H.

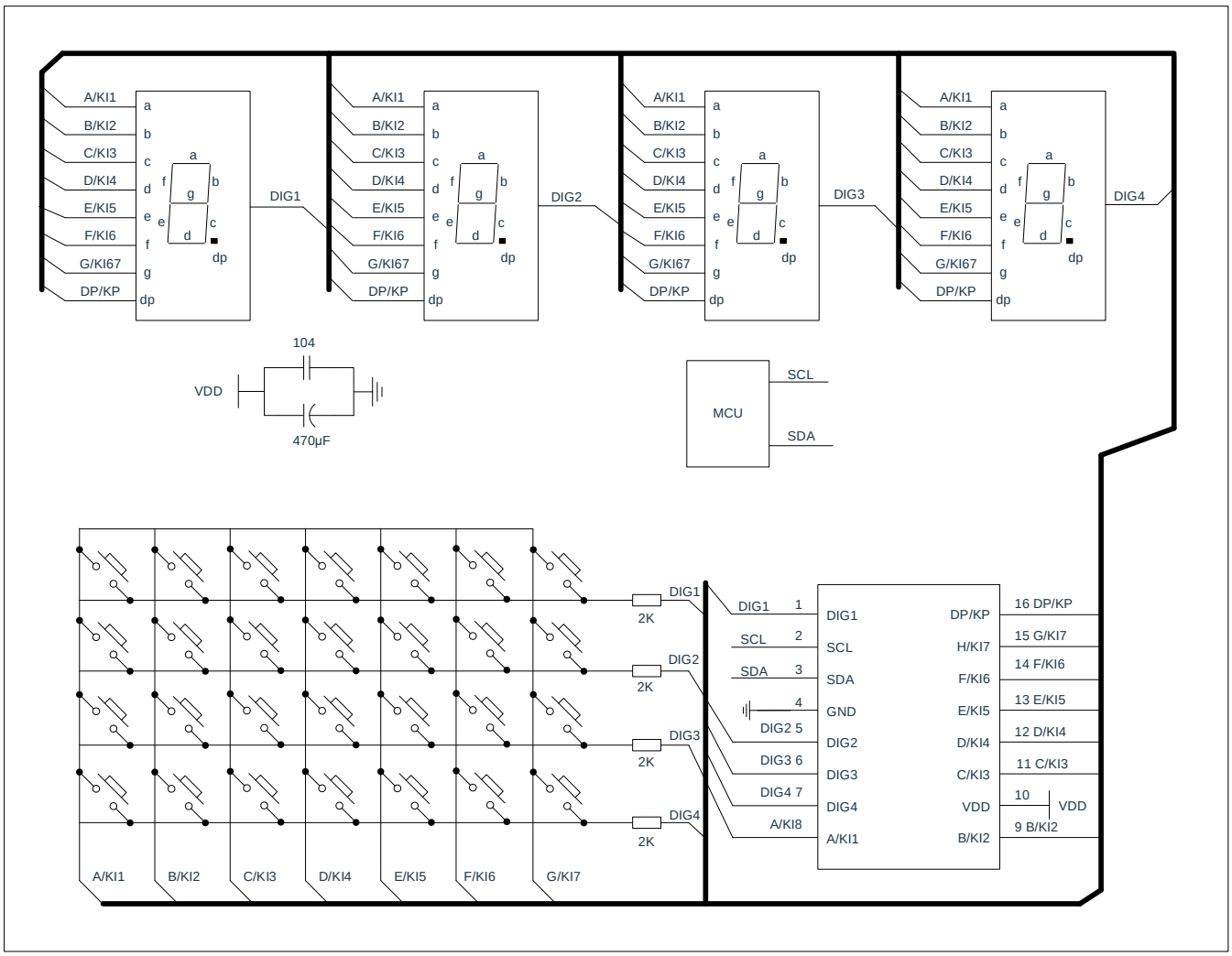
Command2: Turn on the display and set the brightness level.

ADDRESS: Display RAM address.

DATA: Display data.

6. Application Circuit

The wiring circuit diagram for driving a common cathode display with the CMS1650 is shown below.



Note:

1) The filter capacitor for the chip should be placed as close as possible to the CMS1650 pins in PCB wiring to enhance the filtering effect.
2) The traces for the chip's power and ground networks should be as wide as possible. Two 100pF capacitors connected to the SCL and SDA communication ports can reduce interference.
3) Since the forward voltage drop of the blue LED display is approximately 3.0V, a 5.0V power supply should be used for the CMS1650.

7. Electrical Parameters

7.1 Absolute maximum ratings

Symbol	Parameter		Range	Unit
VDD	Logic supply voltage		-0.5～+7.0	V
VIN	Logic input voltage range	SDA, SCL	-0.5～VDD+0.5V	V
Topr	Operating temperature range		-40～+85	℃
Tstg	Storage temperature range		-55～+125	℃
ESD	Human body model (HBM)		3000	V
	Machine model (MM)		200	V

Note:

1) The ratings listed in the table above may cause permanent damage to the device and reduce its reliability under prolonged usage conditions. It is not recommended to operate the chip beyond these limit parameters under any other conditions.
2) All voltage values are measured with respect to the network ground.

7.2 Recommended operating conditions

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
VDD	Supply voltage	-	2.8	5.0	7.0	V
VIH	Input voltage, high	-	0.7VDD	-	VDD	V
VIL	Input voltage, low	-	0	-	0.3VDD	V
TA	Operating ambient temperature	-	-40		+85	℃
TJ	Operating junction temperature	-	-40		+125	℃

7.3 DC characteristics

Unless otherwise specified, test at VDD=3.0V~5.5V and -40℃~+85℃
(test voltage and temperature: VDD=5.0V and TA=+25℃).

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
VDD	Operating voltage		2.8	5.0	7.0	V
IDD	Operating current		0.2		150	mA
ICS	Quiescent current	SCL, SDA, and KP are high		0.2		mA
VIL	Input voltage, low				0.5	V
VIH	Input voltage, high		3			V
VOH	Output voltage, high		VDD-0.4		VDD	V
VOL	Output voltage, low				0.3	V
IOLdig	DIG pin output current, low	VDD=5V, Vo=0.3*VDD		300		mA
		VDD=5V, Vo=0.3V		84		mA
IOHdig	DIG pin output current, high	VDD=5V, Vo=0.7*VDD		18		mA
IOLseg	SEG pin output current, low A~DP	VDD=5V, Vo=0.3*VDD		52		mA
IOHseg	SEG pin output current, high A~DP	VDD=5V, Vo=0.7*VDD		43		mA
		VDD=5V, Vo=VDD-3		58		mA
Rup	KI pin input pull-down resistance	VDD=5V, Vo=0.5*VDD		20		KΩ
	SCL/SDA pull-up resistance	VDD=5V, Vo=0.5*VDD		13		KΩ
VR	Default threshold voltage for power-on reset			2.5		V

7.4 Internal timing parameters

(Test at VDD=5V, T_A= 25℃, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
TPR	Reset time generated by power on detection	10	30	60	ms
TP	Display scanning cycle		7		ms
TKS	Keyboard scanning interval, key response time		40		ms

7.5 Interface timing parameters

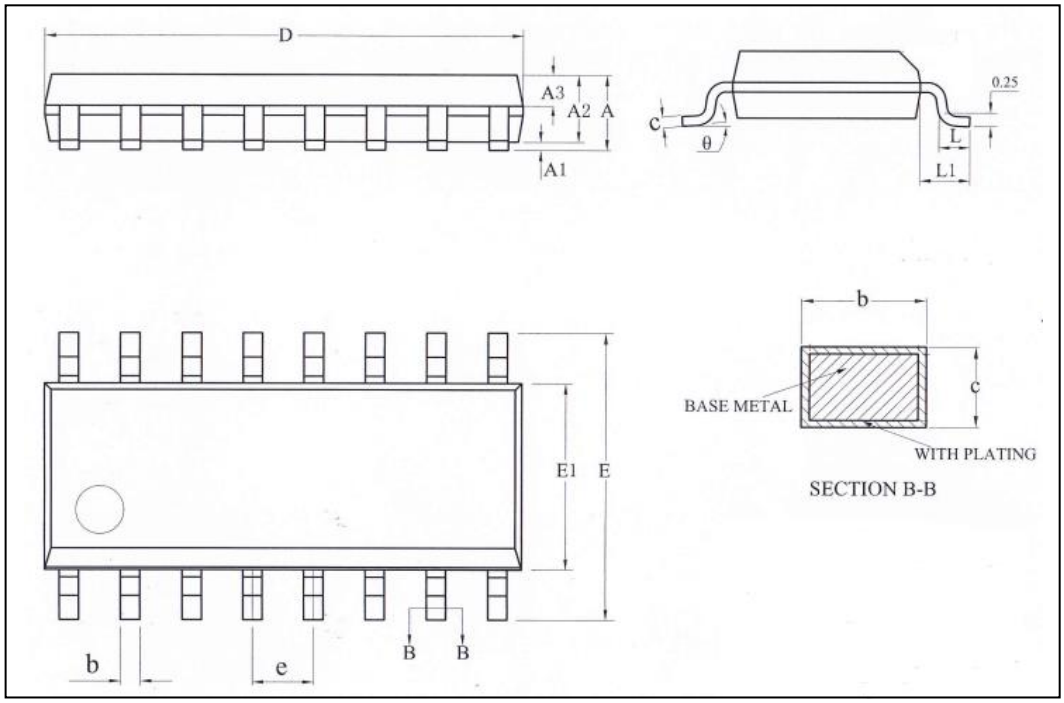
(Test at T_A= 25°C and VDD=5V, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
TSSTA	SDA falling edge start signal setup time	100			ns
THSTA	SDA falling edge start signal hold time	100			ns
TSST0	SDA rising edge stop signal setup time	100			ns
THST0	SDA rising edge stop signal hold time	100			ns
TCLOW	SCL clock signal low level width	100			ns
TCHIG	SCL clock signal high level width	100			ns
TSDA	Setup time of SDA input data to the rising edge of SCL	100			ns
THDA	Hold time of SDA input data to the rising edge of SCL	100			ns
TAA	Delay time of SDA output data valid to the falling edge of SCL	100			ns
TDH	Delay time of SDA output data invalid to the falling edge of SCL	100			ns
Rate	Average data transmission rate			4M	bps

Note: The unit of measurement in this table is nanosecond, i.e. 10^{-9}. If the maximum value is not indicated, the theoretical value can be infinite.

8. Packaging

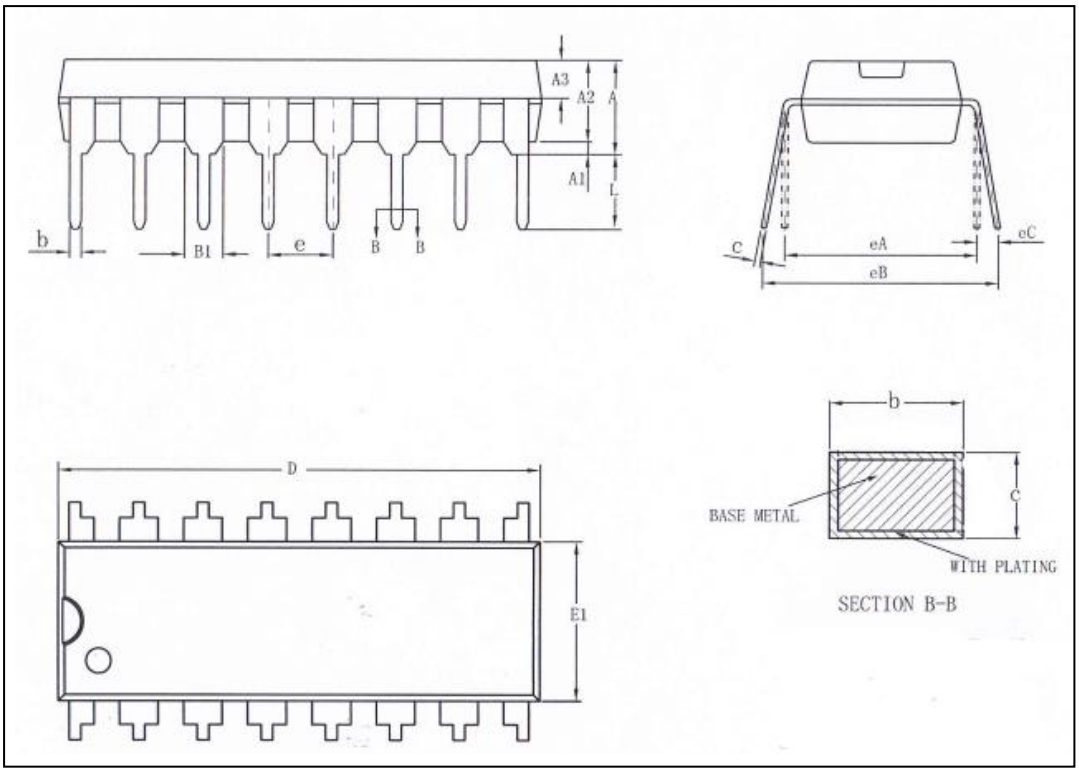
8.1 SOP16



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.85
A1	0.05	-	0.25
A2	1.30	1.40	1.60
A3	0.60	0.65	0.71
b	0.35	-	0.51
c	0.19	-	0.26
D	9.70	9.90	10.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27BSC		
L	0.40	-	0.81
L1	1.05REF		
θ	0	-	8°

Caution: Package dimensions do not include mold flash or gate burrs.

8.2 DIP16



Symbol	Millimeter		
	Min	Nom	Max
A	3.60	-	4.80
A1	0.50	-	-
A2	3.05	-	3.45
A3	1.40	-	1.60
b	0.38	-	0.55
B1	1.52REF		
c	0.21	-	0.35
D	19.00	-	19.40
E1	6.25	6.35	6.45
e	2.54BSC		
eA	7.62REF		
eB	7.62	-	10.90
eC	0	-	1.52
L	2.92	-	-

Caution: Package dimensions do not include mold flash or gate burrs.

9. Revision History

Version	Date	Description of changes
V1.0	May 2019	Initial version
V1.1	November 2021	Updated the format
V1.2	March 2022	Revised the read key data command
V1.3.0	December 2022	Revised pin names of application circuit chips
	September 2024	Modified SOP16/DIP16 package dimensions